CLAIM AMENDMENTS

CLAIMS

1. (presently amended) A fault simulation method for a semiconductor IC, said method comprising the steps of:

generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns of said test pattern sequence, and calculating a logic signal value sequence in each signal line in said semiconductor IC; and

generating a list of faults for each logic gate in said semiconductor IC, which are detectable by a transient power supply current testing using said test pattern sequence, through the use of said logic signal value sequence in said each signal line calculated by said logic simulation, wherein the list of faults is generated by checking, for said each logic gate, whether a logic signal value sequence in an output signal line of said each logic gate has been changed, and if so, generating said fault list in which an identifier of a test pattern sequence having changed said logic signal value sequence and said logic gate are registered in correspondence with each other..

Claims 2 to 4. (canceled)

5. (presently amended) ~~The method of claim 4, wherein said fault list generating step~~ A fault simulation method for a semiconductor IC, said method comprising the steps of:

generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns of said test pattern sequence, and calculating a logic signal value sequence in each signal line in said semiconductor IC; and

generating a list of faults for each signal line, which are detectable by a transient power supply current testing using said test pattern sequence, through the use of said logic

signal value sequence in said each signal line calculated by said logic simulation, wherein said list of faults is generated by:

checking, for said each signal line, whether said logic signal value sequence in said each signal line has been changed; and

if so, checking whether a logic signal value sequence in an output signal line of a logic gate having its input connected to said signal line, in which said logic signal value sequence has been changed, is changed by a test pattern sequence having changed said logic signal value sequence in said signal line, and if so, generating said fault list in which said signal line and an identifier of said test pattern sequence having changed said logic signal value sequence in said signal line are registered in correspondence with each other.

Claim 6. (canceled)

7. (presently amended) ~~The method of claim 6, wherein said fault list generating step is a step of~~ A fault simulation method for a semiconductor IC, said method comprising the steps of:

generating a test pattern sequence composed of two or more test patterns for input to said semiconductor IC;

performing a logic simulation of the operation of said semiconductor IC in the case of applying thereto each of said two or more test patterns of said test pattern sequence, and calculating a logic signal value sequence in each signal line in said semiconductor IC; and

generating a list of faults for each signal propagation path in said semiconductor IC, which are detectable by a transient power supply current testing using said test pattern sequence, through the use of said logic signal value sequence in said each signal line calculated by said logic simulation, wherein said list of faults is generated by checking, for said each signal propagation path, whether logic signal value sequences at respective points in said each signal propagation path have all been changed, and if so, generating said fault list in which an identifier of a test pattern sequence having changed said logic signal value sequences and said each signal propagation path are registered in correspondence with each other.

8. (original claim) The method of claim 1, further comprising the step of calculating said logic signal value sequence for every test pattern sequence prior to said fault list generating step.

9. (original claim) The method of claim 1, further comprising the step of calculating said logic signal value sequence and generating said fault list upon generation of each test pattern sequence.

Claims 10 to 12. (canceled)

13. (new) The method of claim 5, further comprising the step of calculating said logic signal value sequence for every test pattern sequence prior to said fault list generating step.

14. (new) The method of claim 5, further comprising the step of calculating said logic signal value sequence and generating said fault list upon generation of each test pattern sequence.

15. (new) The method of claim 7, further comprising the step of calculating said logic signal value sequence for every test pattern sequence prior to said fault list generating step.

16. (new) The method of claim 7, further comprising the step of calculating said logic signal value sequence and generating said fault list upon generation of each test pattern sequence.